IN-44-CR

311540

P-31

Title: **Laser Annaling of Amorphous/Poly: Silicon Solar Cell Material Flight Experiment**

Type: **Final Technical Report**

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Period: **Oct. 89 - June 90**

Grantee: **George Mason University**
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Grant Number: **5-26051, NAG 5- 1294**

Code 724, Eric Cole (GMU)

MICROELECTRONICS MATERIALS PROCESSING EXPERIMENT

by

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[1.0] INTRODUCTION

This paper outlines the preliminary design being proposed for the microelectronics materials processing experiment. It includes an overall mission profile, description of all processing steps, analysis methods and measurement techniques, data acquisition and storage and a preview of the experimental hardware as currently defined.

The goal of this project is to investigate the viability of material processing of semiconductor microelectronics materials in a micro-gravity environment. The two key processes being examined are:

1. Rapid Thermal Annealing of Semiconductor Thin Films and Damaged Solar Cells

2. Thin Film Deposition using a Filament Evaporator

The Rapid Thermal Annealing (RTA) process will be used to obtain higher quality crystalline properties from amorphous/poly-Si films. For a more detailed discussion of this process, refer to the proposal submitted.

RTA methods can also be used to repair radiation-damaged solar cells. On earth this technique is commonly used to anneal semiconductor films after ion-implantation. The damage to the crystal lattice is similar to the defects found in solar cells which have been exposed to high-energy particle bombardment.

Also under investigation is the behavior of a thin-film deposition process using a filament evaporator. The effects of the micro-gravity environment on the deposition and grain quality of various samples is to be studied.

[1.1] MISSION PROFILE

Figure 1.1 illustrates the overall mission profile from the standpoint of the materials processing experiment. Appropriate figures regarding each phase of the mission are included in the illustration.

NOTE: The parameters indicated represent the current best estimate regarding power, duration, energy and time. They indicate the upper bound in most cases.

Figure 1.1

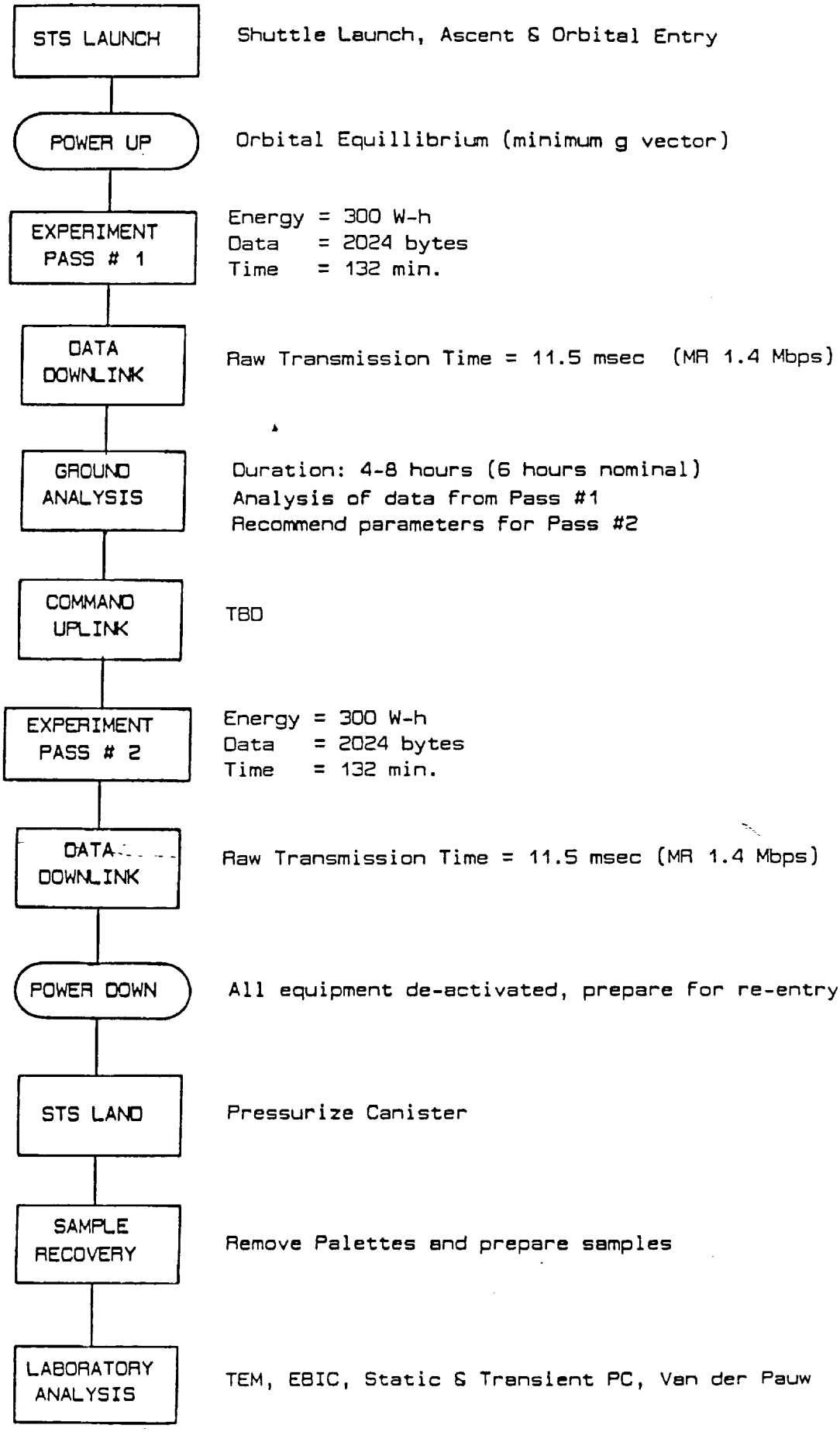
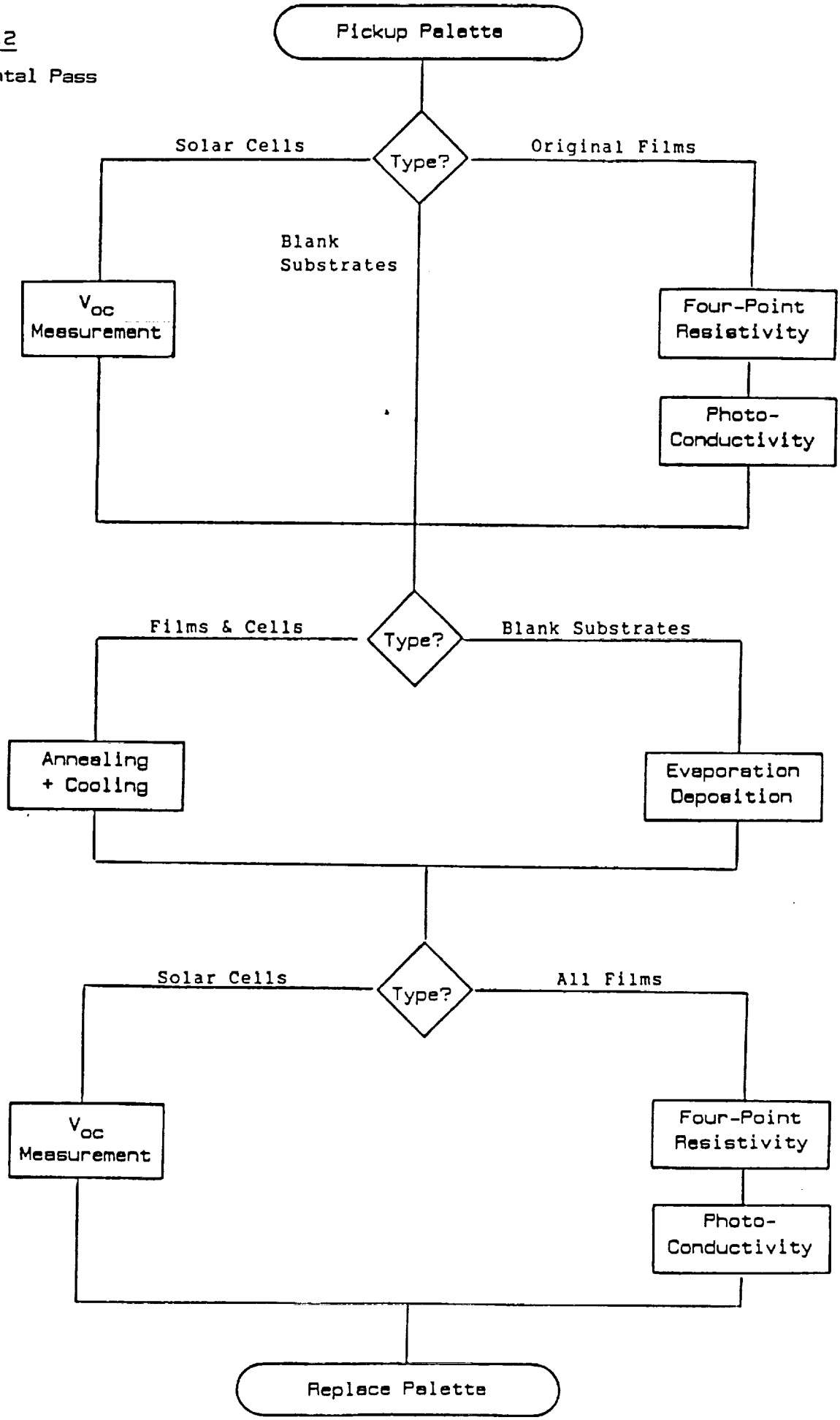

STS LAUNCH
Shuttle Launch, Ascent & Orbital Entry
POWER UP
Orbital Equillibrium (minimum g vector)
EXPERIMENT PASS # 1
Energy = 300 W-h
Data = 2024 bytes
Time = 132 min.
DATA DOWNLINK
Raw Transmission Time = 11.5 msec (MR 1.4 Mbps)
GROUND ANALYSIS
Duration: 4-8 hours (6 hours nominal)
Analysis of data from Pass #1
Recommend parameters for Pass #2
COMMAND UPLINK
TBD
EXPERIMENT PASS # 2
Energy = 300 W-h
Data = 2024 bytes
Time = 132 min.
DATA DOWNLINK
Raw Transmission Time = 11.5 msec (MR 1.4 Mbps)
POWER DOWN
All equipment de-activated, prepare for re-entry
STS LAND
Pressurize Canister
SAMPLE RECOVERY
Remove Palettes and prepare samples
LABORATORY ANALYSIS
TEM, EBIC, Static & Transient PC, Van der Pauw

Figure 1.2

Experimental Pass



[2.0] ANNEALING PROCESS

The lamp annealing procedure is performed in a custom-made furnace. The heating element is a quartz Halogen lamp in combination with a mono-ellipsoidal reflector. The furnace design is shown in Figure 2.1 . In addition, two thermocouples are used along with the required electronics to measure the temperature profile during the annealing process. The robot manipulator is required to position the sample palette (4 samples per palette) in a 3" by 1" open "window" at the bottom plate of the furnace. The positioning accuracy required is estimated at +/- 1mm. Once the annealing is complete, the lamp power is shut off, allowing the samples to cool by radiation. After cooling down to the GAS can's ambient temperature (defined as 0°C for shuttle in Earth-Viewing Mode), the manipulator disengages the palette from the window frame. Figure 2.2 outlines the annealing process.

[2.1] Control Method

The power/temperature and duration of the anneal is preset for each group of 4 samples in a palette. Two Cr-Al Type K thermocouples (one serves as backup) are used to sample the furnace temperature once every second during the process. When the temperature reaches a preset value (T_{max}) the lamp power is cutoff. As a safety feature, the power is automatically shut off after the set duration for the anneal, in case the temperature sensors should fail. Therefore the process is regulated in the so-called 'Peak Temperature Control Mode', with a preset maximum duration.

[2.2] Process Parameters

The process parameters for each group of 4 samples are stored in the flight VAX control program. The first 16 samples will be processed according to these stored parameters while the second pass of the experiment will process the remaining 16 samples according to the recommended parameters uplinked from ground control after analyzing the data obtained in the first pass.

The parameters for this process consist of the setpoint temperature (T_{max}), maximum duration and the expected cooldown period.

Figure 2.1

Furnace
Cross Section

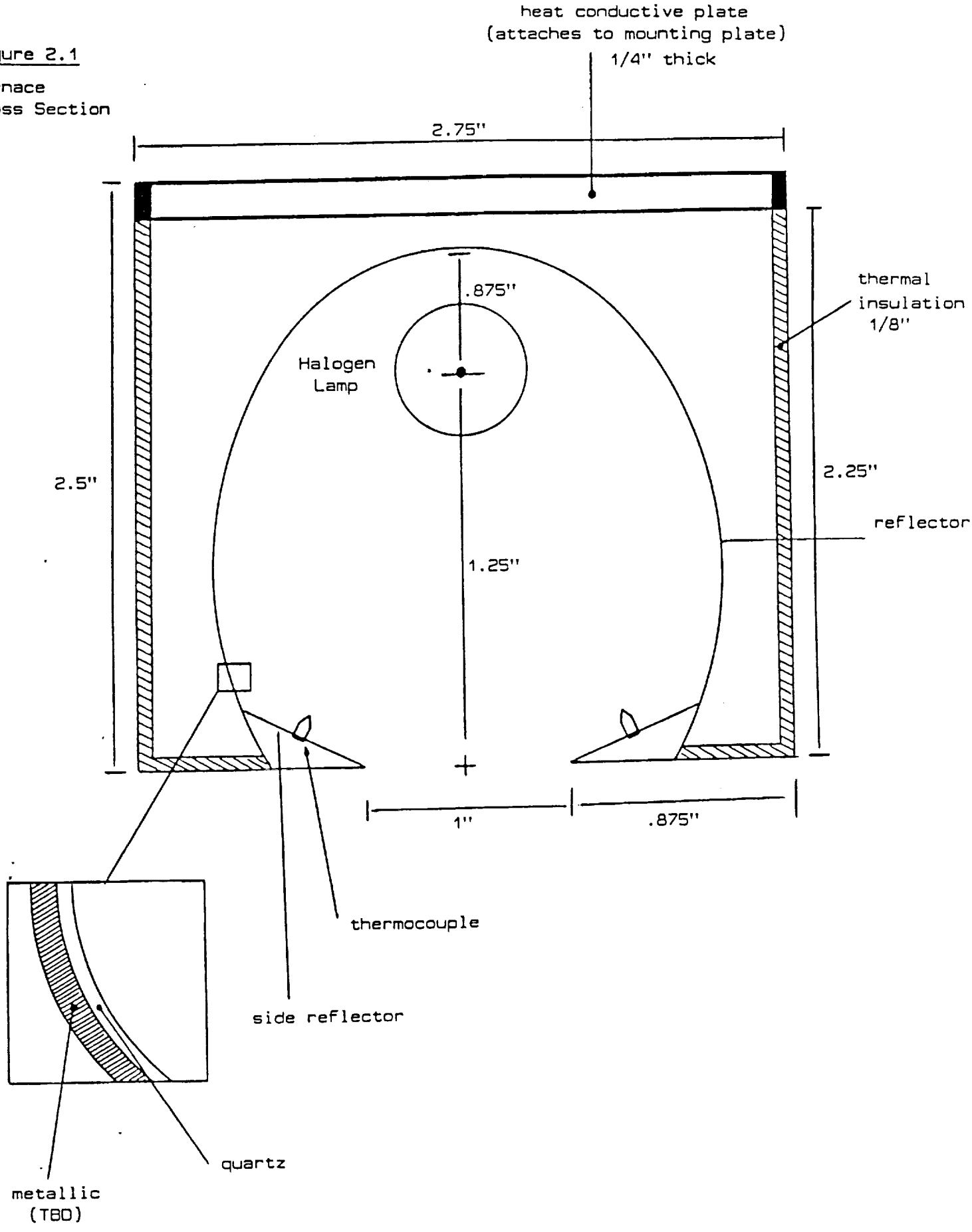
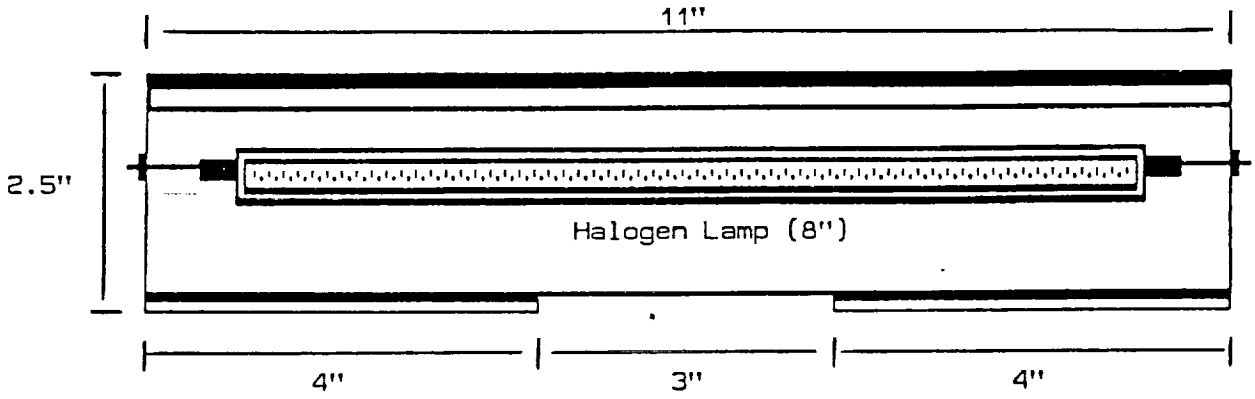


Figure 2.1 (cont.)

Furnace Side View



Furnace Bottom View

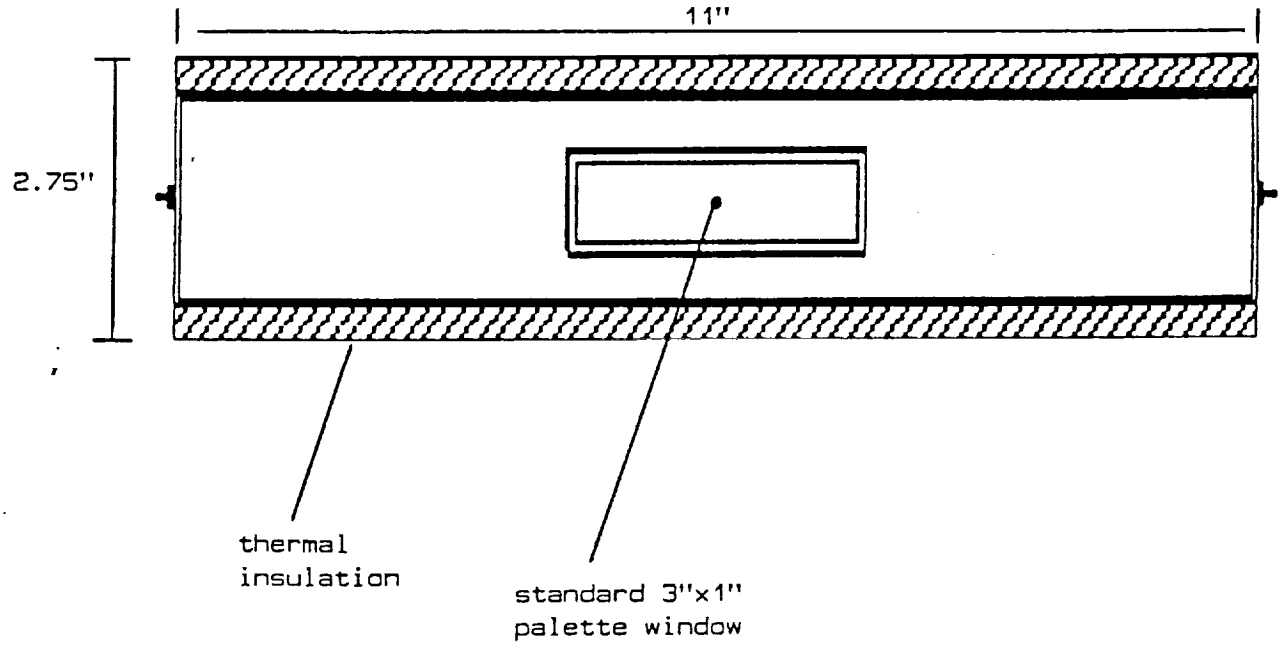
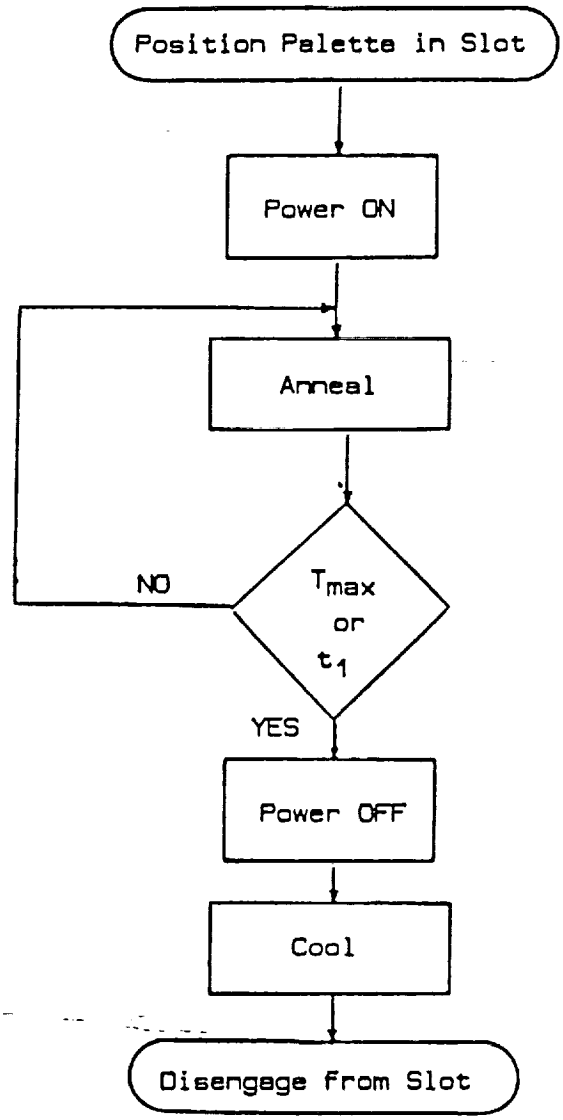
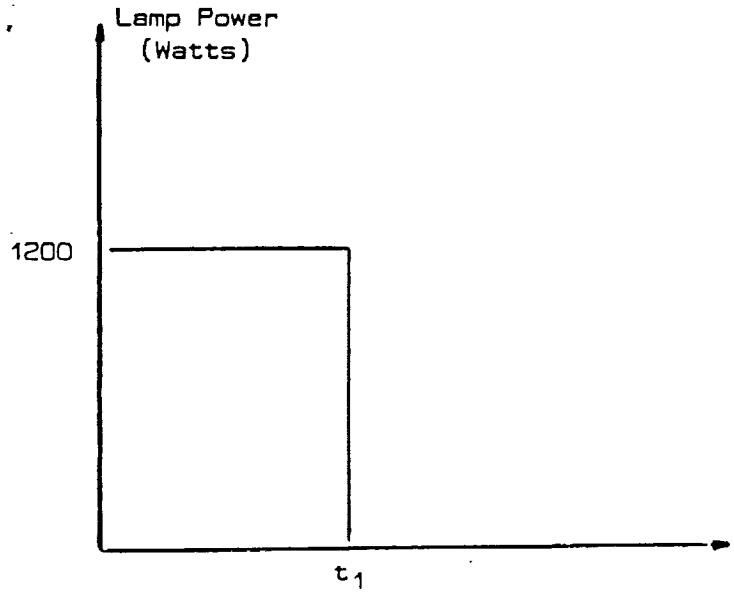
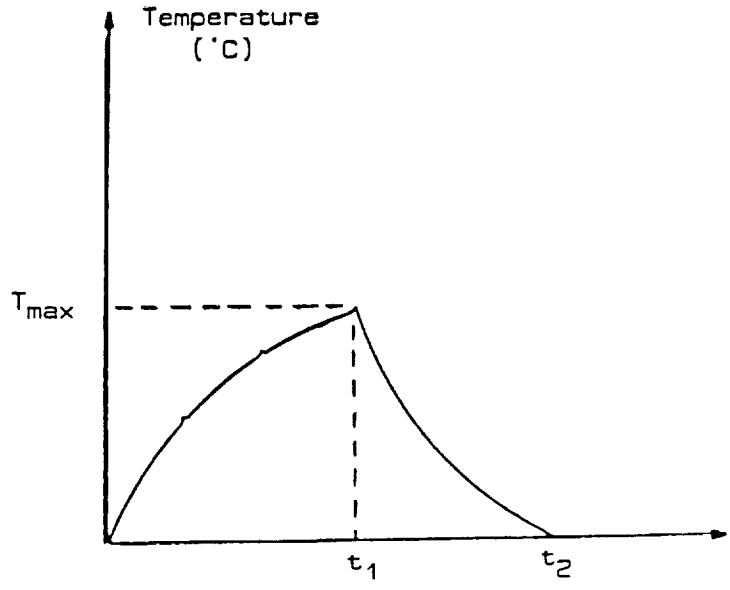


Figure 2.2

Annealing Procedure







Semiconductor Films

* Lamp Power ... 1200 Watts
* Peak Temperature ... 1300 °C
* Max. Duration ... 3 mins.
* Cooling Time ... 1 min.
* Energy Usage ... 60 Watt-Hours
* Total Time ... 5 mins.

Solar Cells

* Lamp Power ... 1200 Watts
* Peak Temperature ... 300 °C
* Max. Duration ... 45 secs
* Cooling Time ... 1 min.
* Energy Usage ... 15 Watt-Hours
* Total Time ... 3 mins.

[] Total Mission Energy Use: 270 Watt-Hours

for 4 semiconductor film palettes (60 Wh per palette)
and 2 solar cell palettes (15 Wh per palette)

[2.3] Data Acquisition

The temperature is to be sampled at a rate of 1 Hz for the maximum duration of the anneal (5 mins) and the data is to have an accuracy of +/- 1°C. The temperature samples are to be stored in 2-byte data words.

[] Total Mission Memory Use: 3600 bytes

for a total of 6 palettes (600 bytes per palette)

[] Total Mission Time Use: 30 mins.

for a total of 6 palettes (5 mins. per palette)

[3.0] DEPOSITION PROCESS

In this process a filament evaporator is used to deposit thin films of silicon on a variety of substrates. The evaporation takes place inside an evacuated chamber with a standard 3" x 1" opening to allow the palette to engage the chamber. Figure 3.1 shows the chamber's geometry. The procedure is outlined in Figure 3.2 .

* Filament Power ... 1200 Watts (30 VAC, 30-40 Amps, 60 Hz)
* Evaporation Time ... 3 mins.
* Filament Material ... Tungsten (coated with Si)
* Filament Length ... 2"
* Filament Diameter ... 1/2"
* Energy Usage ... 60 Watt-Hours

This experiment requires no measurements and consequently no data is gathered. However it must be performed during orbital equillibrium (min. g vector). A total of 2 palettes (ie. 8 sample substrates) will be processed in this way.

[] Total Mission Energy Use: 120 Watt-Hours

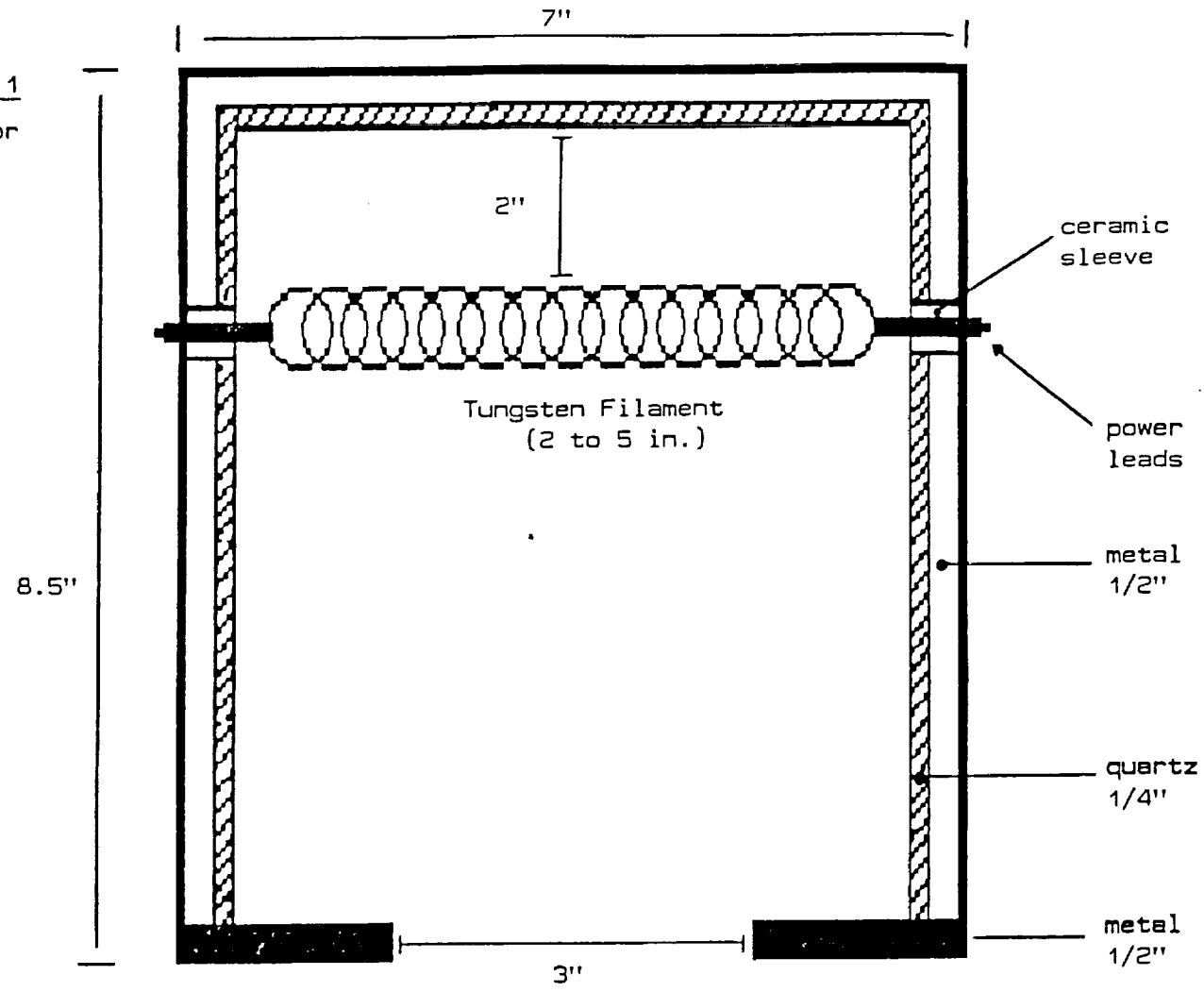
For a total of 2 palettes (60 Wh per palette)

[] Total Mission Time Use: 10 mins.

For a total of 5 mins. per run (3 mins evaporation + 2 mins. cooldown) and a total of 2 palettes to be processed

Figure 3.1

Evaporator Chamber



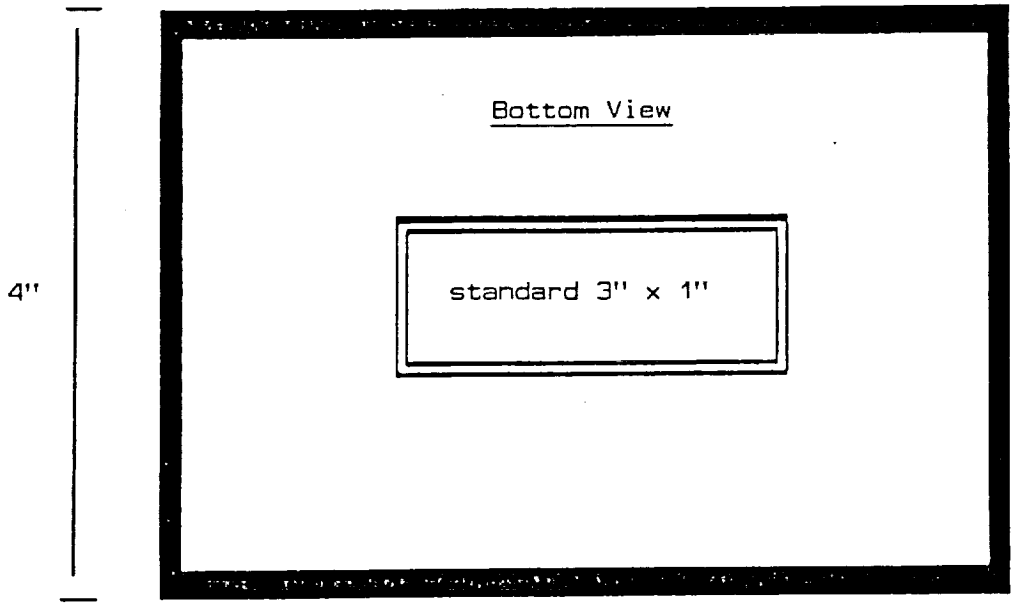
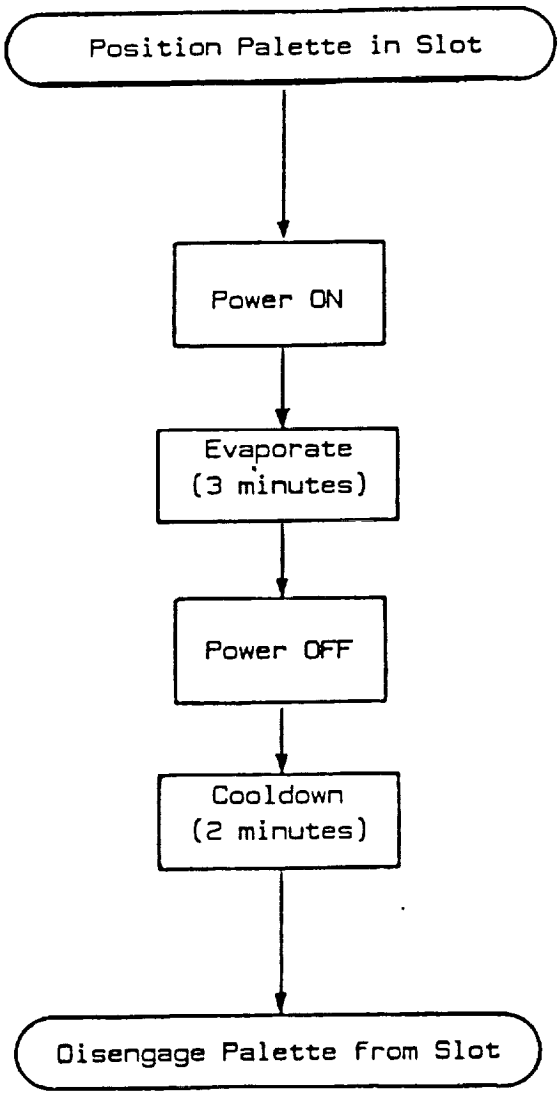


Figure 3.2

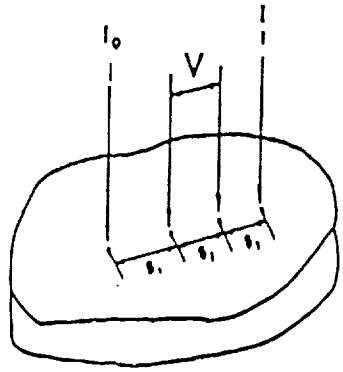
Deposition Cycle



NOTE: Since this process is solely time-controlled, a safety measure must be introduced. For example, in the case of the filament shorting out, the power circuitry could be designed to shut off filament power when it reads a sudden increase in current. Similarly, zero current (dead filament) can also trigger power cutoff. This would then signal an ABORT condition to the main controller (Flight VAX).

[4.0] RESISTIVITY ANALYSIS

The resistivity of semiconductor films can be used as a measure of the crystalline quality both before and after the thermal annealing process. Lattice defects, impurities and discontinuity in the short and long-term order of the sample can be gauged with the measurement of the bulk surface resistivity. The rapid thermal annealing of the original films is expected to yield larger grain sizes in a micro-g environment. Hence an increase in the measured resistivity is anticipated following the thermal annealing process.



The most popular method for measuring the resistivity of a sample is the four-point probe method shown above. Although various geometries are possible the most commonly used is the in-line four-point method illustrated. A constant current source is used to pass a known value of current through the outer two probes while a sensitive voltmeter measures the voltage appearing across the two inner probes. Different probe spacings can be used although the equations are simplified for the case of uniform spacing:

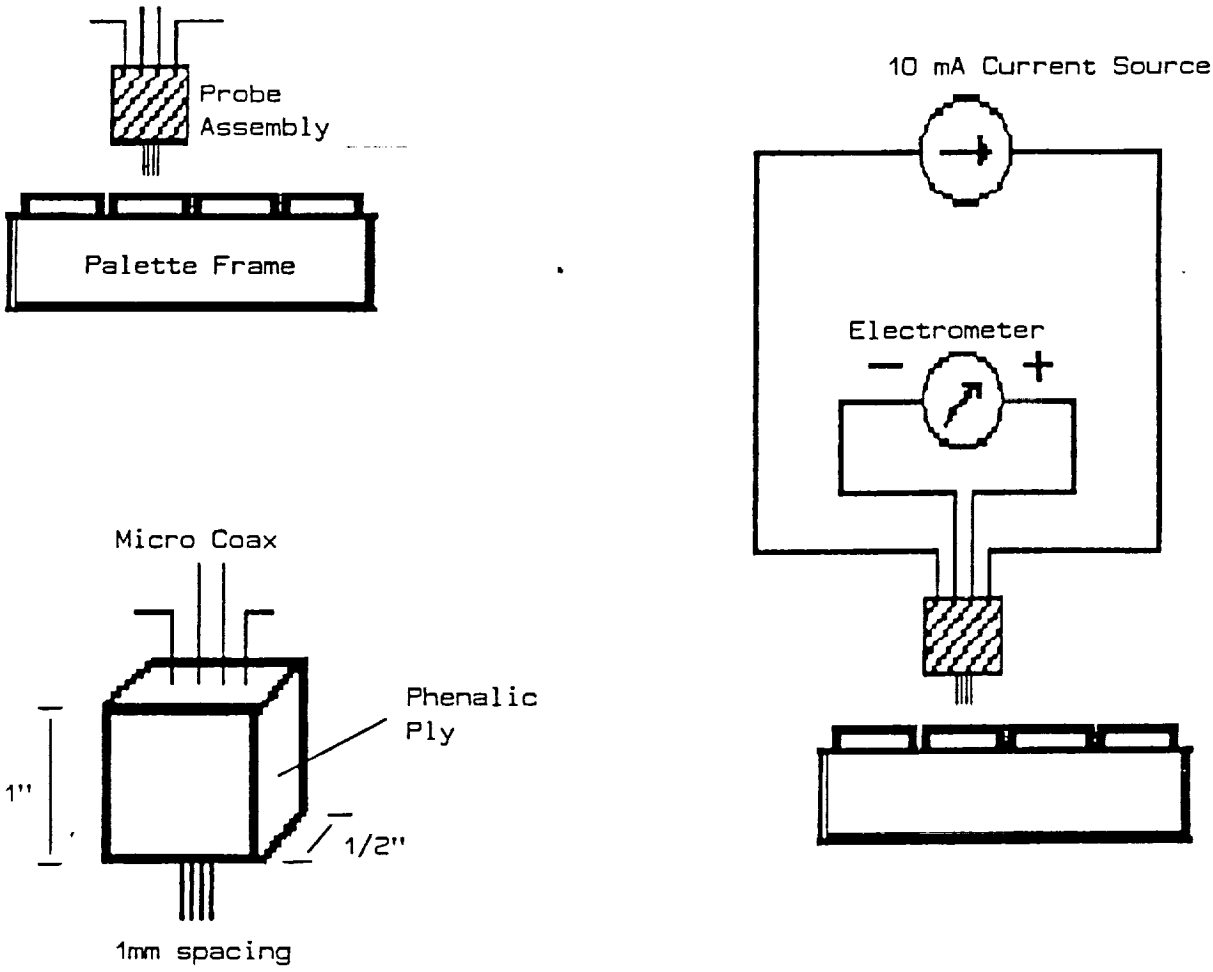
$$\text{Resistivity} = 2\pi(V/I)\ [\ 1/S_1 + 1/S_3 - 1/(S_1 + S_2) - 1/(S_2 + S_3)\ ]$$

which simplifies to the following equation for the case of equal spacing,

$$\text{Resistivity} = 2\pi S\ (V/I)$$

In reality, there are a variety of correction factors which must be included to obtain a true measure of the surface resistivity of the material being examined.

[4.1] Four-Point Probe



The probe assembly consists of Au-tipped, spring-loaded metallic probes with a 1mm spacing. A 10mA constant current source is used to apply the outer probe current while a sensitive electrometer is used to measure the voltage (typical range: 1uV - 1mV). The probe housing is mounted against the inside wall of the canister. Consequently the robot manipulator must translate the palette to measure all 4 samples. In order to insure a good electrical contact the manipulator must apply a 1.0lb force maintained while the sample is being measured. All electronics measuring hardware is mounted on the HH-plate, outside the GAS canister. Extra four-point probes will be available in case of damage during operation.

[4.2] Analysis Procedure

1. Position Palette under four-point probe station (position accuracy of +/- 1mm)
2. Engage four-point probe (apply 1 lb force)
3. Power up 10mA current source
4. Sample voltage reading (repeat 60 times during 1 min. and average voltage)
5. Compute Resistivity using V/I and stored correction factors
6. Store Resistivity value in Data Page (in memory)
7. Turn off current source
8. Disengage palette/sample from probes
9. Move to next sample

[4.3] Data Acquisition

* The Final value of Resistivity computed will have 6-digit precision
* Format: 32-bit IEEE Floating-Point (7-digit mantissa)

[] Total Mission Power Use: minimal (instrument power consumption TBD)

[] Total Mission Memory Use: 192 bytes
for 24 samples, before & after and with 4 bytes per measurement

[] Total Mission Time Use: 96 min.
for 24 samples, before & after and with 2 min. per measurement

[4.4] Specifications

* Keithley Electrometer w/ GPIB standard interface
  Power: TBD
  Voltage: 115 VAC, 60 Hz
  Dimensions: 3" by 5" by 10"
  Weight: 1.5 lbs.

* Keithley Current Source (rated to 100mA with +/- 1%)
  Power: TBD
  Voltage: 115 VAC, 60 Hz
  Dimensions: 4" by 5" by 6"
  Weight: 2.0 lbs.

[5.0] PHOTOCONDUCTIVITY ANALYSIS

The photoconductivity of a semiconductor sample is a valuable measure of the crystal quality. Larger grain sizes obtained by the thermal processing result in reduced carrier trapping (due to a reduced overall grain boundary surface area). As trapping sites decrease in density throughout the material, the mean carrier lifetimes increase.

The direct method of measurement involves analyzing the decay in photoconductivity as pulse of light (typical duration 0.1 usec) is flashed on the sample. The sub-band gap light source results in the photo-generation of electron-hole pairs and momentarily increases the conductance. However typical decay lifetimes range in the nano-seconds and are difficult to measure. Furthermore a great deal of data would have to be stored and transmitted if a typical decay cycle was to be sampled.

Therefore, a simpler measurement technique is used to obtain the lifetimes of the carriers using a static photoconductivity test. In this method a CW light source with band-gap wavelength is used to illuminate the sample, while a steady current measurement is taken. For poly/amorphous Si with a band-gap energy of ~ 1.8 eV, the optimum wavelength of the light source is 690nm. Although pure-spectral sources (lasers) are best, this experiment uses a 100 Watt Halogen lamp with a spectrum covering the appropriate range. Two Au-tipped probes with a 1mm spacing are used to apply an electric field to the sample while a series electrometer measures the steady-state photo-current I_p .

$$I_p = ne\ u\ (V/d)\ lt$$

where n is the free electron photogenerated density, e is the electronic charge, u is the drift mobility, V is the applied voltage, d is the probe gap, l is the probe length and t is the sample thickness. The value of free electron density is given by:

$$n = t_n F(1-R)[1-\exp(-at)]/t$$

where t_n is the carrier lifetime, F is the photon emission rate (which can be computed from the incident power absorbed), R is the surface reflectivity and a is the absorption coefficient. Most of the above parameters can be determined with reasonable accuracy for the samples being tested. Since mobility itself is a function of photo-generated carrier concentration, it is possible to use the above equations to compute a lifetime-mobility product from a measurement of the current. This will be indicative of the measure of new performance obtained after the thermal annealing process.

[5.1] Analysis Procedure

Figure 5.1 illustrates the probe geometry for the experiment. The 100W halogen lamp is housed inside the upper structure of the probe assembly. The light source is filtered and focused by the glass/lens aperture which also contains the probe wiring and the tips. The entire assembly will be mounted against the inside wall of the GAS canister, therefore the robot manipulator is required to translate the palette as required to contact all 4 samples on a palette.

1. Position Palette under probe assembly (accuracy +/- 5mm)
2. Engage sample with probe (apply 1lb force)
3. Turn on 100W halogen lamp (focused on sample)
4. Raise applied voltage (0 to 10 volts)
5. Measure photo-current (repeat 60 times over a 1 min. period and average)
6. Compute lifetime-mobility product using stored parameters and coefficients
7. Store product
8. Turn off voltage & lamp
9. Disengage from probe
10. Move on to nest sample

[5.2] Data Acquisition

* The experiment stores one computed value for the lifetime-mobility product or alternatively, a photo-current value.

* Format: 32-bit IEEE Floating-Point (7-digit precision)

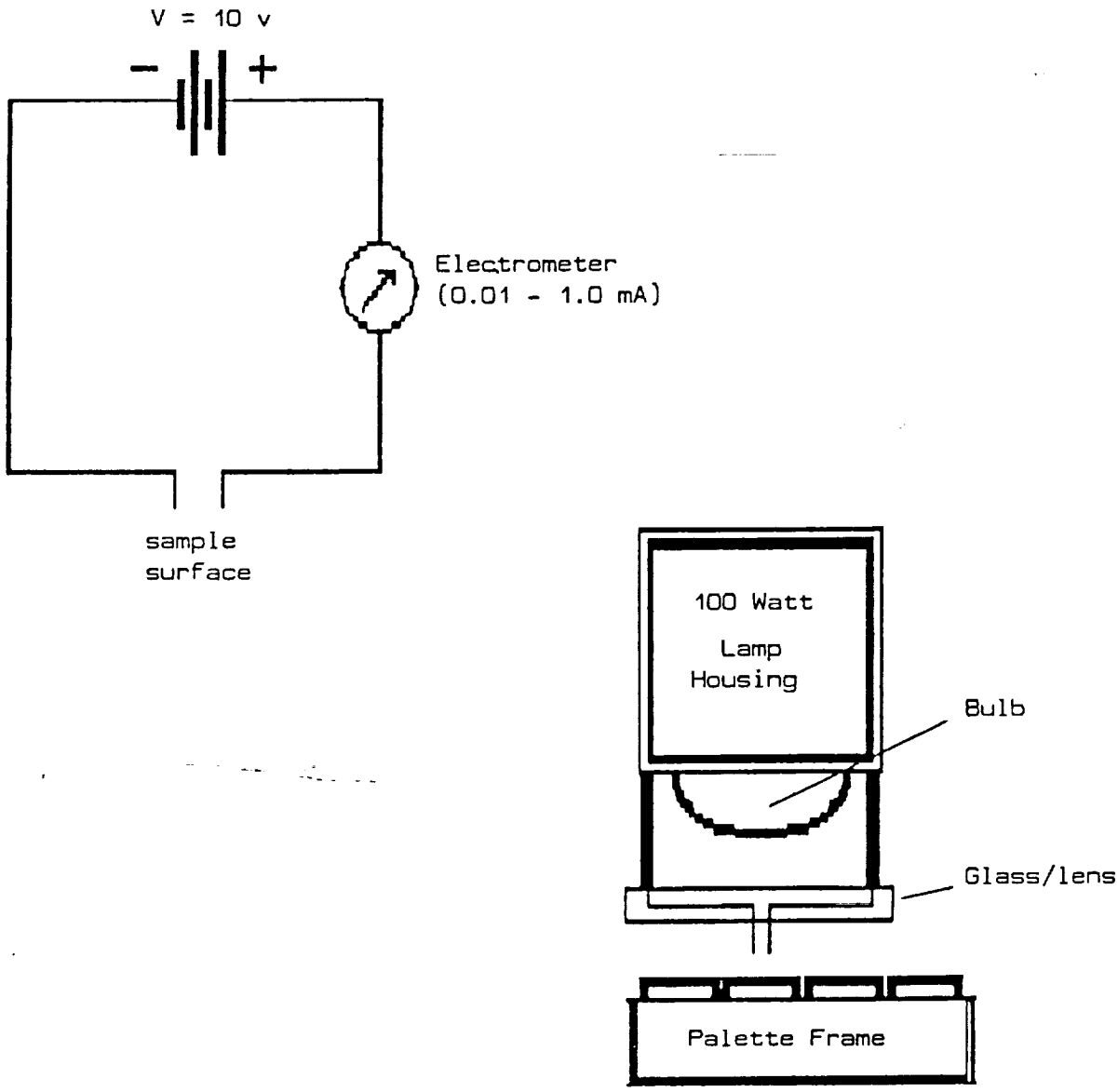
[] Total Mission Energy Use: 160 Watt-Hours
for 24 samples, before and after process (2 min. per run)

[] Total Mission Memory Use: 192 bytes
for 24 samples, before and after process (4 bytes per measurement)

[] Total Mission Time Use: 96 min.
for 24 samples, before and after process (2 min. per run)

Figure 5.1

Photoconductivity
Test Station



[6.0] SOLAR CELL ANALYSIS

For the 8 solar cell samples to be taken aboard the experiment module, only one analysis technique will be used. This is the open-circuit voltage measurement which is characteristic for solar cells. A special two-point probe shown in Figure 6.1, is used to simultaneously contact both the back metal contact of the cells and the grid metal fingers on the surface. Both probes are spring loaded, to provide contact with the metal with variable applied force/pressure. A similar 100 Watt halogen lamp is used to illuminate the cells while the probes measure the open-circuit voltage which develops across the pn junction in the cell.

[6.1] Analysis Procedure

1. Position palette under probe assembly (+/- 2mm accuracy)
2. Engage sample with probe (apply 1lb force)
3. Turn on 100W Halogen lamp
4. Measure Voltage (repeat 60 times for 1 min. and average)
5. Store Voltage value
6. Turn off lamp power
7. Disengage palette from probe
8. Move on to nest sample

[6.2] Data Acquisition

* One voltage measurement per sample to be stored as a 32-bit IEEE FP data word

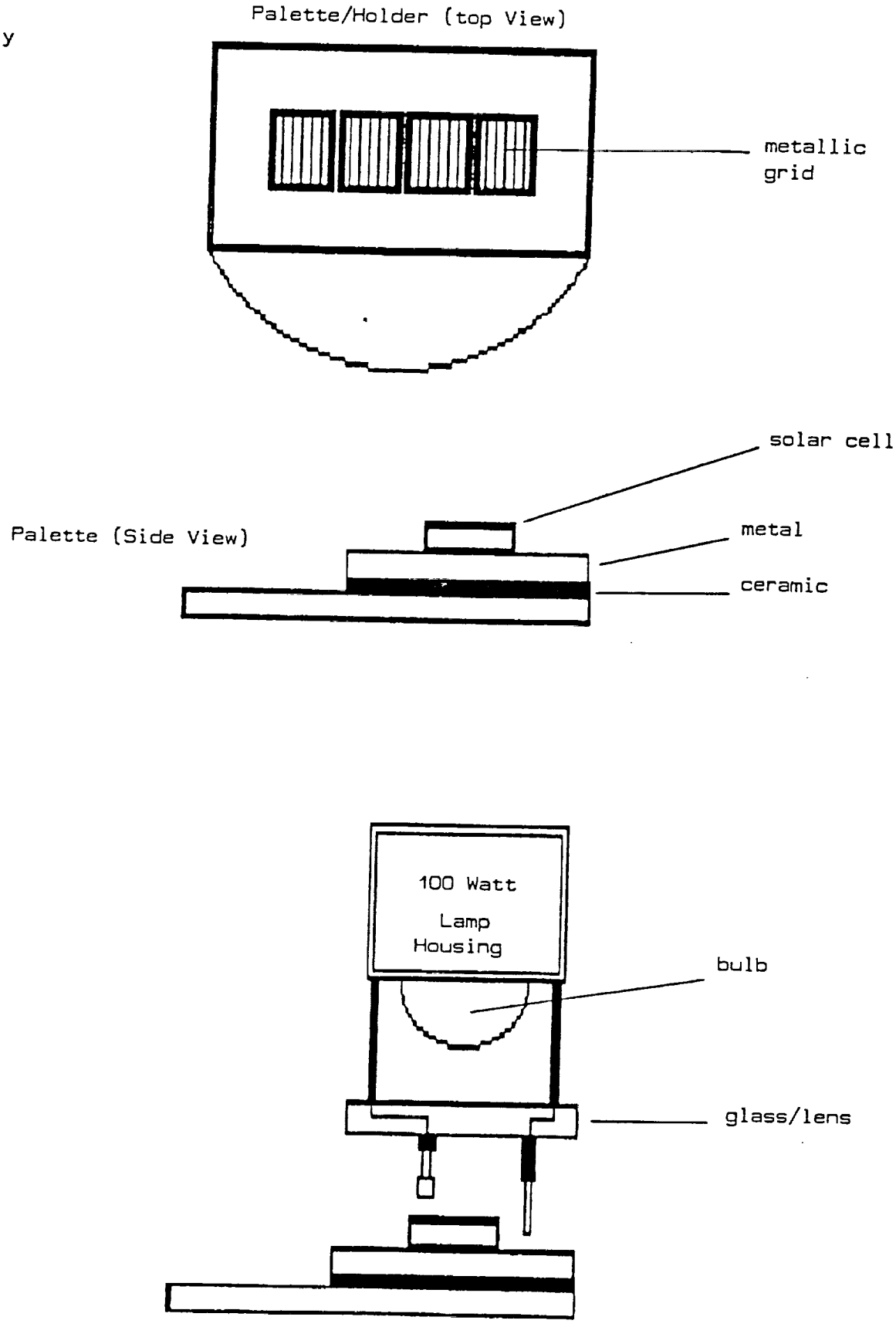
[] Total Mission Energy Use: 53 Watt-Hours
for 8 samples, measured before & after (2 min. per run)

[] Total Mission Memory Use: 64 bytes
for 8 samples, measured before & after (4 bytes per measurement)

[] Total Mission time Use: 32 min.
for 8 samples, measured before & after (2 min. per run)

Figure 6.1

Open-Circuit
Voltage
Test Assembly



[6.3] Specifications

NOTE: The specifications for the open-circuit voltage test are similar to those mentioned in 5.3 .

[7.0] SAMPLES

As already mentioned each palette (sample holder) contains 4 samples. The overall collection of samples for this project are as follows:

* 2 Solar Cell Palettes
* 2 Substrate Palettes
* 2 Free-Standing Palettes (quartz frame)
* 2 Additional Palettes (Silicon frame)

[] Total = 32 samples (in 8 palettes)

16 samples processed in Pass #1
16 samples processed in Pass #2 (after command uplink of new process parameters)

[] Sample Sizes:

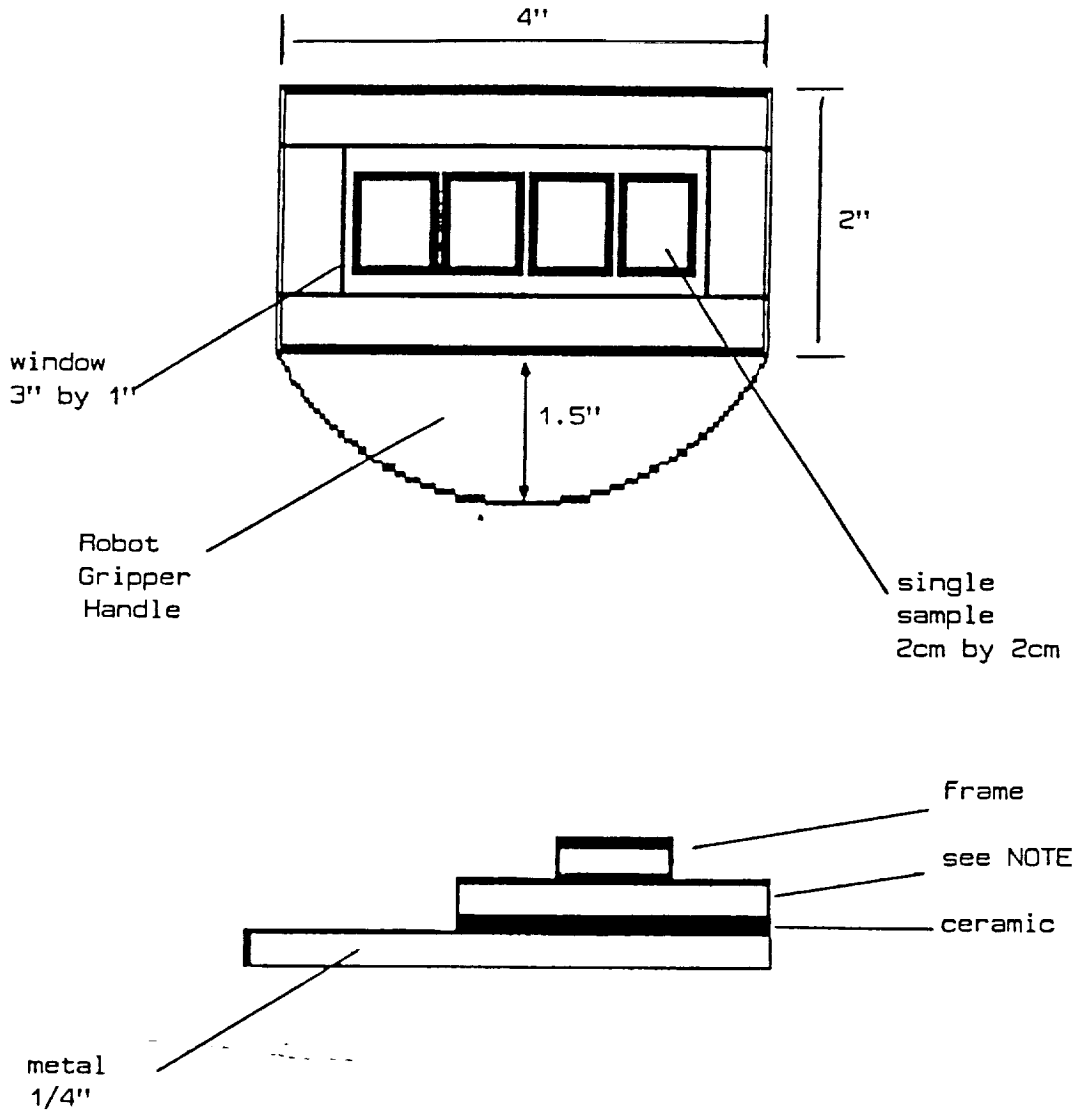
- Films: 2cm by 2cm by 100-400 microns
- cells: 2cm by 2cm by 100 mils
- subs : 2cm by 2cm by 100 mils

[8,0] SAMPLE HOLDER/PALETTE

The standard palette is designed to allow the robot to grasp the holder and manipulate it in the GAS can environment. The group of 4 samples on a plate are arranged in the frame structure on the palette. The dimensions of this frame are: 2.9" by 0.9" and is so designed as to fit into the standard 3" by 1" window opening in both the annealing furnace and the evaporation chamber. Please refer to the following figures.

Figure 8.1

Palette
Design



NOTE: This layer depends on the type of samples being carried on the plate.

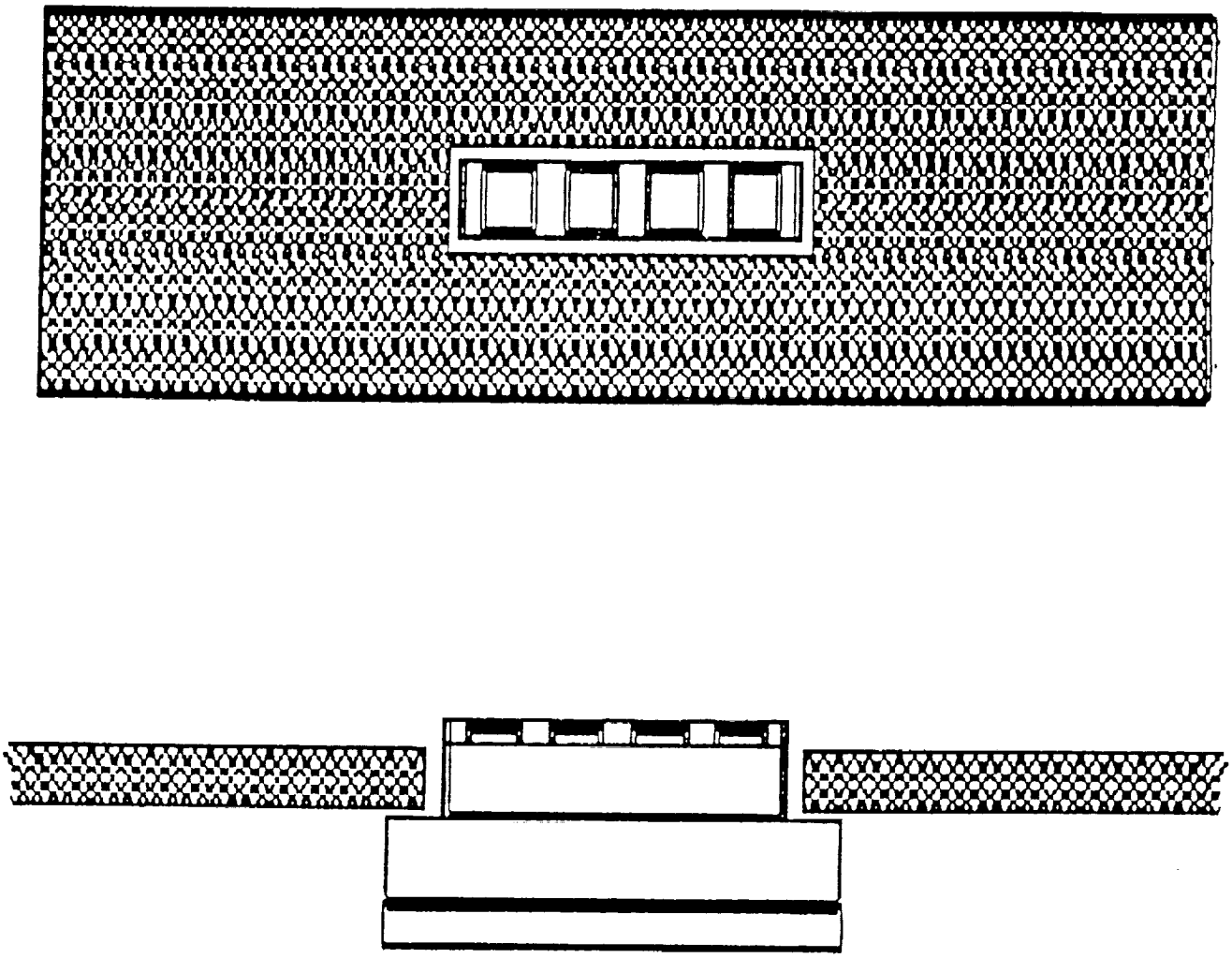
For films:	ceramic	1/8-1/4" thick
For subs :	metal	(thickness depends on sample TBD)
For cells:	metal	(thickness depends on sample TBD)

Also note that this layer is metal for solar cells and hence provides an ohmic contact with the cells' back plate which acts as an electrode.

Figure 8.2

Palette Fit
in standard

3" by 1" window



* Sample frames can be attached to the ceramic or metal layer on the palette in the following ways:

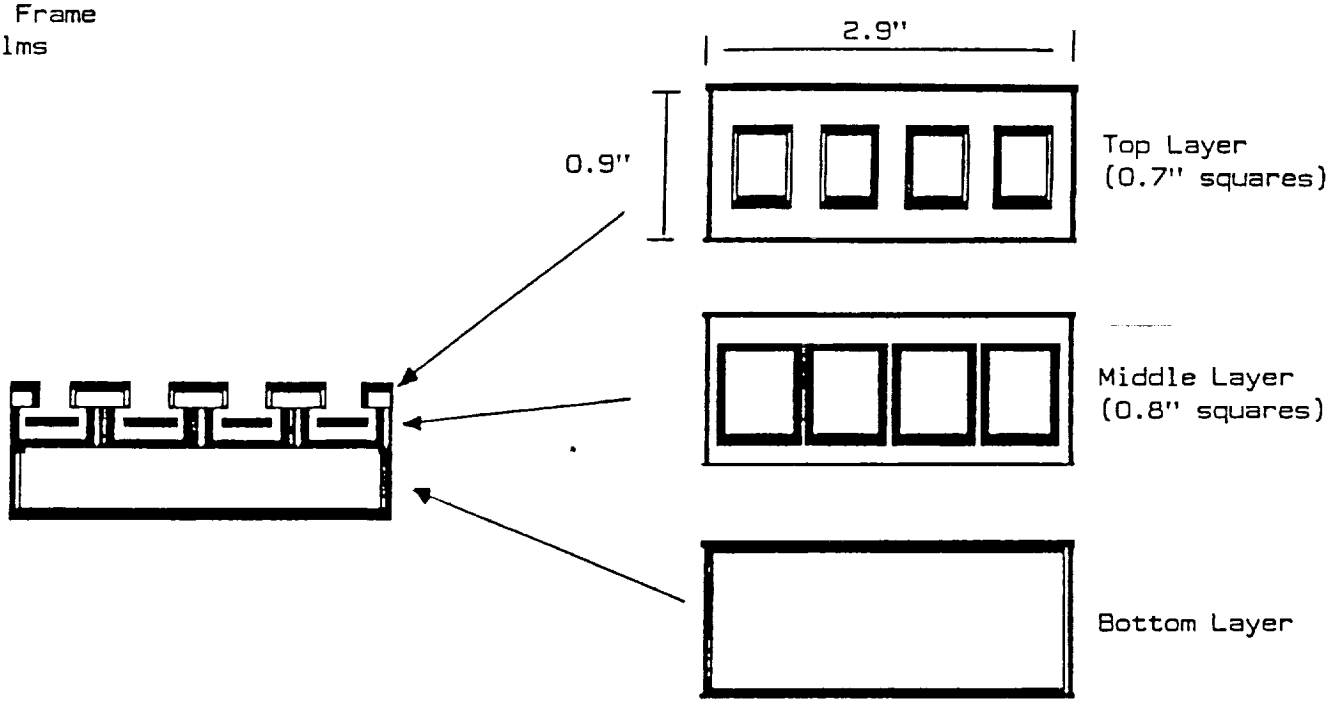
- Cells: welded, soldered or pressure-held with clips (on metal layer)
- Subs : epoxied, glued down or pressure-held with clips (on metal layer)
- Films: glued or clipped on ceramic layer

NOTE: There are two types of frames for film samples:

1. Free-standing quartz frame
2. Silicon frame (w/ SiN)

Figure 8.3

Quartz Frame
for Films



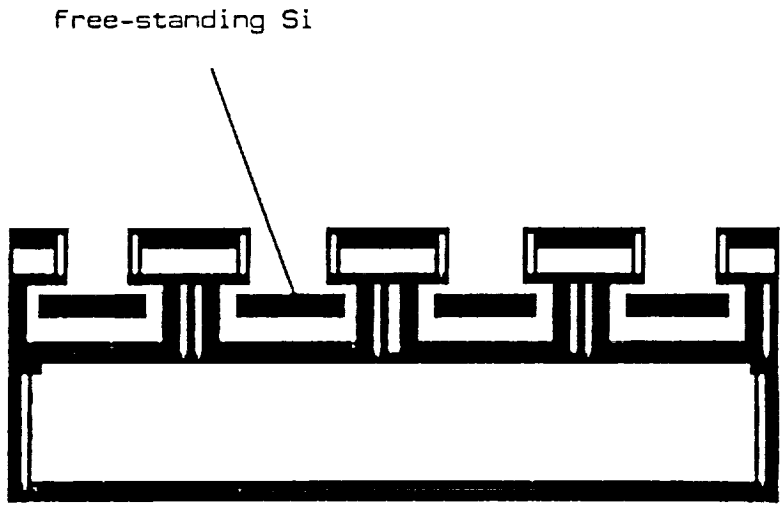
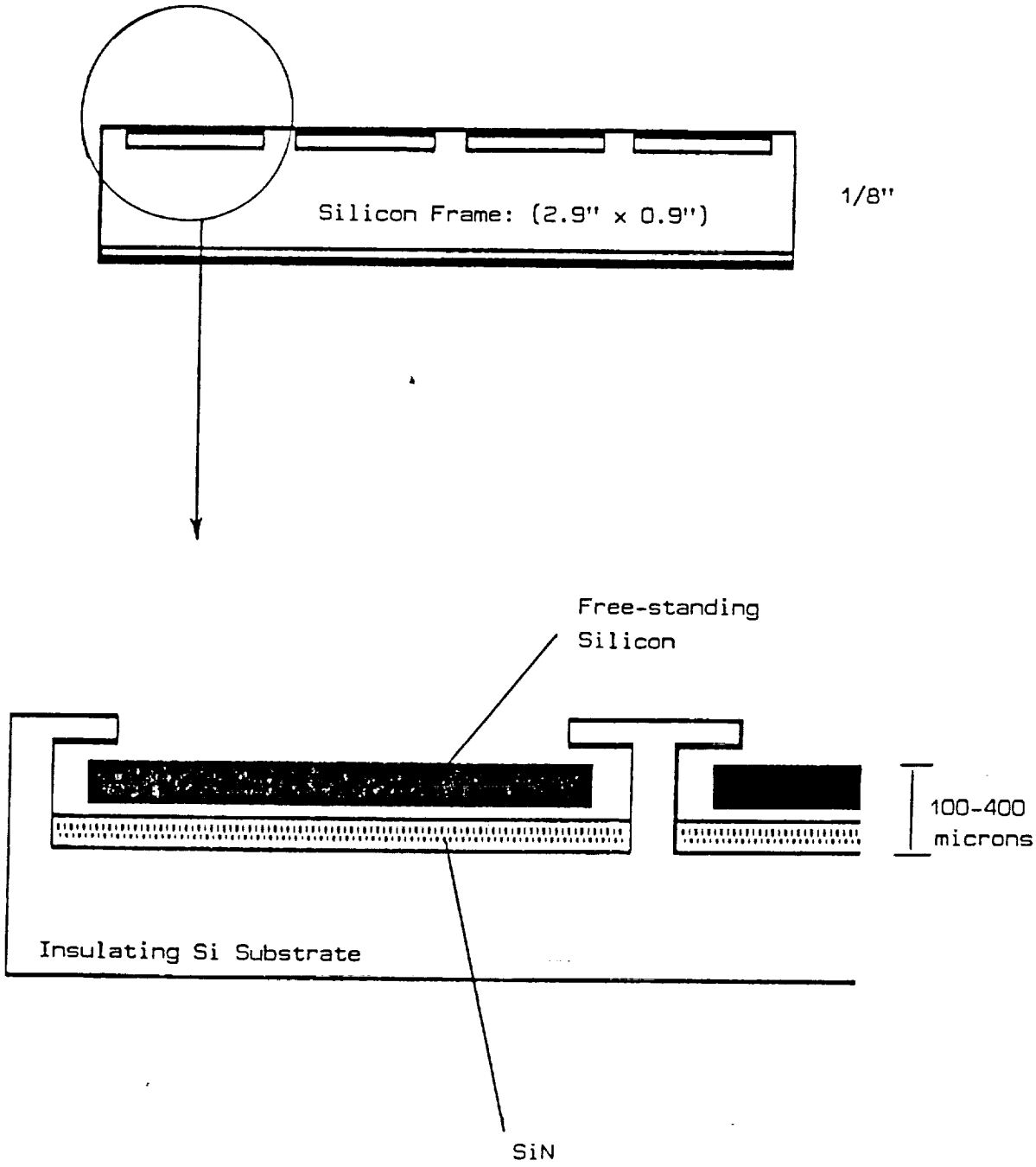


Figure 8.4

Si Frame
For Films



[9.0] GAS CANISTER DESIGN

Figure 9.1 shows the preliminary GAS can overall design. The two annealing furnaces and the 2 evaporation chambers are located in opposite quadrants at the very top level of the canister. The top plate of these experiment modules are attached to the canister's mounting plate and provide for heat dissipation via conduction through the un-insulated top plate.

The mid-level portion of the canister is partially occupied with the analysis modules. This consists of at least 3 probe station corresponding to the resistivity, photoconductance and the open-circuit voltage test. In reality this equipment is attached to the main structure which is bolted to the top mounting plate of the canister.

The bottom level is the sample hold area. At the current time, 32 samples are being considered which are carried on 8 palettes. There is additional room in this level for placing a video-camera station for taking B & W snapshots of the samples or for monitoring the operation of the robot manipulator.

NOTE: The GAS canister is to be evacuated to a pressure of 10^{-5} Torr for all of the experiments and processes conducted. The canister is pressurized to 1 atm after the orbiter has landed and the payload is ready to be removed.

[10.0] PROBLEMS

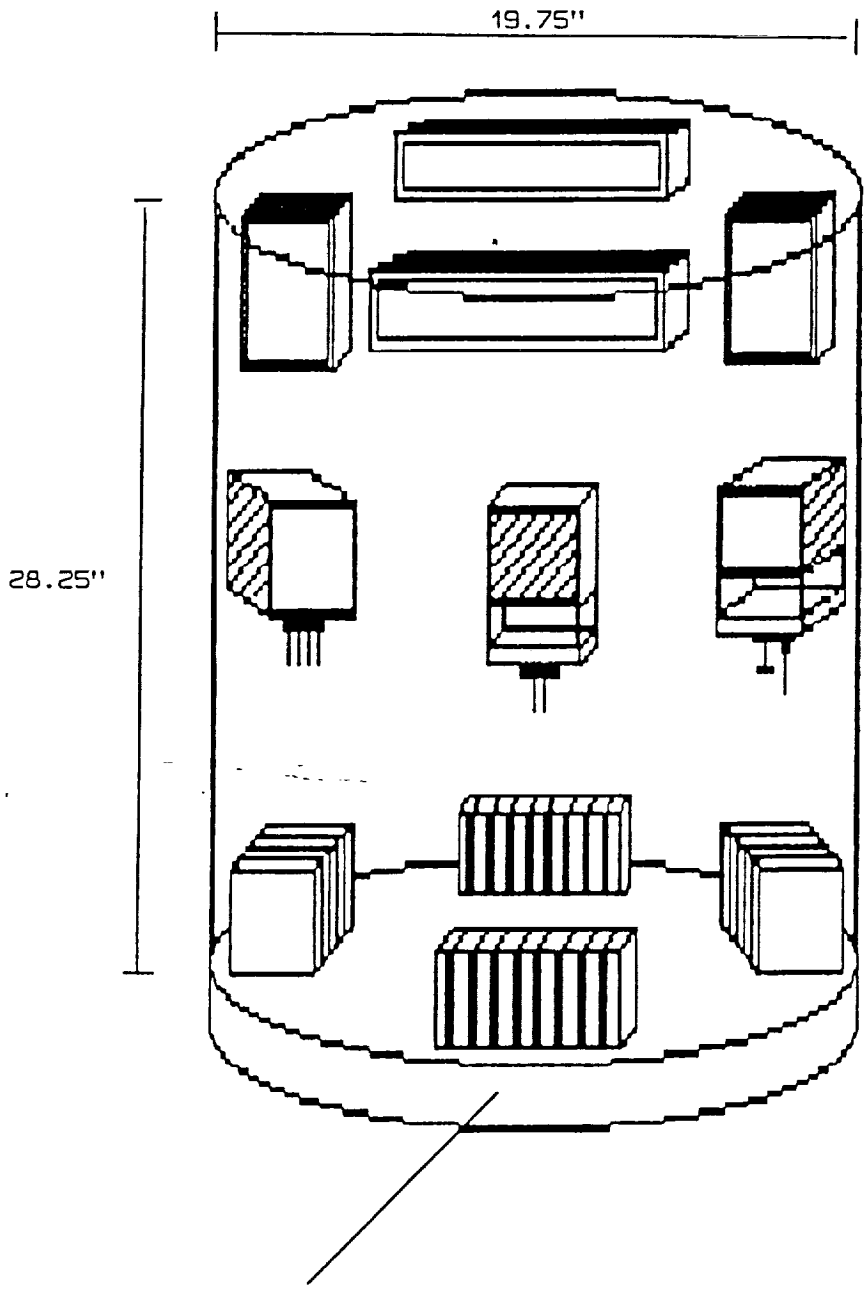
* Can adequate power conditioners be used to provide the necessary current and voltage for all the equipment?

* Is the heat dissipation through the top plate sufficient to allow rapid cooldown after heating processes?

* All lamp heating procedures must be tested for proper operation under the high temperatures encountered during the experiments. Possibility of bulb failure?

Figure 9.1

Preliminary
GAS Canister
Design



[] Thin-Film Deposition of a-Si on Various Substrates

In addition to the main annealing re-crystallization process, the deposition of a-Si on various substrates has been proposed. This method will use filament evaporation to deposit thin films of amorphous Si (.5-1 micron) on an assortment of substrates. Since such experiments in a micro-g environment have been limited, the potential for growing uniform epitaxial layers of a-Si with relatively little defects should be explored. Similar techniques have been used on earth to deposit crystalline and polycrystalline n and p-type Si on glass (conducting), steel and other cheap substrates.

Among the many factors related to this process, the choice of a low-cost substrate is one of the most important. The material used should exhibit :

1. Low cost
2. Low electrical resistance
3. The thermal coefficient of expansion should match that of the Si layer closely over the entire deposition temperature range.
4. No impurities should diffuse in the overlying Si layer.
5. Substrate should have large grain size inorder for the deposited Si to have the same. Grain boundaries of substrate will be present in the epitaxial layer.

Candidate substrate material have been extensively studied by [Chu] and some of them along with the problems encountered in their use are tabulated below:

MATERIAL	PROBLEM AREAS
Carbon	Grain size, impurities
Graphite	Grain size, impurities
Sapphire (Al_2O_3)	Price, insulator
Steel (w/ diffusion barrier)	Grain size, impurities, thermal expansion
Upgraded Metallurgical-grade Si (UMG-Si)	Impurities

Consequently [Chu] has found that UMG-Si is indeed the best suited material for use as substrate in solar cells. This material is obtained starting with 98% pure MG-Si reduced from quartz by carbon. Subsequently MG-Si is further purified by acid-leaching to a level of 99.9% and them crystallized by Czochralski pulling.

The advantage of UMG-Si is its relatively low cost compared to other substrates used in solar cells. The upgrading of MG-Si ($1/Kg.) is a fast and low-cost process and results in a substrate material which is cost-efficient. Furthermore, the junction formed between the UMG-Si substrate and the deposited amorphous Si will be in essence a homojunction thus resulting in reduced discontinuities and trapping states. In particular, the crystalline nature of UMG-Si should contribute to the formation of larger grain sizes in the deposited poly or amorphous film layer (as in property 5 stated earlier).

Once the impurity atoms have been removed from UMG-Si (B and Al being the most concentrated of the impurities present) this material should be a very attractive choice for solar cell substrates. A reduction in the crystallographic defect density in the epitaxial layers had been demonstrated and a solar cell efficiency of 12.9% was obtained with single-crystal UMG-Si and as high as 10.3% on polycrystalline material. Therefore epitaxial deposition on a UMG-Si substrate can yield a low cost slice since the substrate is obtained wihtout the expensive and energy-consuming Siemens process. Before acid leaching the MG-Si only costs $1/Kg. compared to the electronic-grade Si which costs $50/Kg.. It is estimated that with continued research in this area, the epitaxial deposition on UMG-Si could yield wafer costs as low as $1.00/W [Overstraeten].

Chu T L et al , Proceedings of the 12th Photovoltaic Specialists Conference /1976, New York: IEEE , p. 74

Overstraeten R J Van, Mertens R P, Physics, Technology and Use of Photovoltaics , Adam Hilger Ltd., Bristol & Boston, 1986, pp. 120-125